Vendor: ARM

Exam Code: EN0-001

Exam Name: ARM Accredited engineer

Version: Demo

QUESTION NO: 1

In a Cortex-A9 processor, when the Memory Management Unit (MMU) is disabled, which of the following statements is TRUE? (VA is the virtual address and PA is the physical address)

A. VA == PA; No address translations; instructions and data are not cached
B. VA! = PA; No address translations; instructions may be cached but not data
C. VA == PA; Address translations take place; data may be cached but not instructions
D. VA == PA; No address translations; instructions may be cached but not data

Answer: D

QUESTION NO: 2

In the Generic Interrupt Controller (GIC), when an interrupt is requested, but is not yet being handled, it is in which of the following states?

A. Inactive
B. Active
C. Pending
D. Edge-triggered

Answer: C

QUESTION NO: 3

A simple system comprises of the following memory map:

Flash - 0x0 to 0x7FFF

RAM - 0x10000 to 0X17FFF

When conforming to the ABI, which of the following is a suitable initial value for the stack pointer?

A. Top address of RAM (0x18000)
B. Top address of flash (0x8000)
C. Bottom address of RAM (0x10000)

D. Bottom address of flash (0x0000)

Answer: A

QUESTION NO: 4

A program running on a development board that is connected to a host using a debugger can access a file on the host by using:

A. Memory mapping
B. Semihosting
C. Polling
D. Virtual I/O

Answer: B

QUESTION NO: 5

In which type of storage will the compiler preferentially place frequently accessed variables?

A. Stack
B. Heap
C. Registers
D. Hard disk

Answer: C

QUESTION NO: 6

What view in a debugger displays the order in which functions were called?

A. The Call Stack view
B. The Memory view
C. The Registers view
D. The Variables view

Answer: A

QUESTION NO: 7

Printf statements could be used to achieve which of the following debug tasks?

A. Observe changes to a local variable in a function
B. Capture a real-time trace of program execution
C. Debug boot code, before a call to the C main() function
D. Stop the processor at an interesting location in the code

Answer: A

QUESTION NO: 8

When the processor is executing in Thumb state, which of the following statements is correct about the values stored in R15?

A. Bits[31:16] are duplicated with bits[15:0]
B. The PC value is stored in bits[31:1] and bit[0] is treated as zero
C. The PC value is stored in bits[31:16] and bits[15:0] are undefined
D. The PC value is stored in bits[15:0] and bits[31:16] are undefined

Answer: B

QUESTION NO: 9

A standard performance benchmark is being run on a single core ARM v7-A processor. The performance results reported are significantly lower than expected. Which of the following options is a possible explanation?

A. L1 Caches and branch prediction are disabled
B. The Embedded Trace Macrocell (ETM) is disabled
C. The Memory Management Unit (MMU) is enabled
D. The Snoop Control Unit (SCU) is disabled

Answer: A

QUESTION NO: 10

When setting the initial location of the stack pointer and the base address of the heap, the ARM EABI requires that the:

A. Base address of the heap must be the same as the initial stack pointer.
B. Stack pointer must be 8-byte aligned.
C. Heap must be in external RAM.
D. Initial stack pointer must be the lowest addressable memory location.

Answer: B

QUESTION NO: 11

In an ARMv7-A processor, which control register is used to enable the Memory Management Unit (MMU)?

A. The ACTLR
B. The SCTLR
C. The TTBCR
D. The CONTEXTIDR

Answer: B

QUESTION NO: 12

A simple method of measuring the performance of an application is to record the execution time using the clock on the wall or a wristwatch.

When is this method INAPPROPRIATE?

A. When executing the software using a simulation model

B. When the processor is a Cortex-R4
C. When instruction tracing is enabled
D. When the processor is not executing instructions from cache

Answer: A

QUESTION NO: 13

Consider the following code sequence, executing on a processor which implements ARM Architecture v7-A.

LDR r0, [r1]

STR r0, [r2]

STR r3, [r3]

R1 points to a location in normal memory. R2 and R3 point to device memory.

Which of the following statements best describes the ordering rules which apply to this sequence?

A. The two writes to device memory will happen in program order, but the read can be performed out of order
B. The memory accesses can happen in any order
C. The memory accesses will happen in program order
D. The read to r0 and the write from r0 will happen in program order, but the write from r3 can be performed out of order

Answer: C

QUESTION NO: 14

When using the default ARM tool-chain libraries for bare-metal applications. I/O functionality is rerouted and handled by a connected debugger. This is often referred to as semihosting. Which one of the following explanations BEST describes how this feature can be implemented by a debugger?

A. The library directly sends I/O requests to the debugger using the JTAG connection
B. While the target is running, the debugger processes I/O requests from a shared queue in

memory
C. The I/O library calls rely on an Ethernet connection to redirect the requests to the debugger
D. The I/O library calls generate an exception that is trapped and handled by the debugger

Answer: D

QUESTION NO: 15

The Cortex-A9 processor implements a feature called "small loop mode" which reduces power consumption when executing small loops by turning off instruction cache accesses. Which of the following statements describes a condition that must be satisfied for this mode to be enabled?

A. The loop must fit into two cache lines
B. The loop must only contain forward branches
C. Only integer arithmetic can be used
D. All variables must be held in registers

Answer: A

QUESTION NO: 16

Which is the best power saving mode to use while waiting to obtain a lock on a semaphore?

A. Dormant
B. Standby
C. Shutdown
D. Deep sleep

Answer: B

QUESTION NO: 17

Which privileged mode can kernel code use to get direct access to the User mode registers R13 and R14?

A. Abort mode
B. System mode
C. Hypeivisor mode
D. Supervisor mode

Answer: B

QUESTION NO: 18

An Advanced SIMD intrinsic has the prototype:

int16x4_t vmul_n_s16(int16x4_t a, int16_t b);

How many multiplications does this intrinsic compute?

A. 1 multiplication
B. 4 multiplications
C. 16 multiplications
D. 64 multiplications

Answer: B

QUESTION NO: 19

Which of the following memory attributes, specified in a translation table entry, could be used to protect a page containing a read-sensitive peripheral from speculative instruction fetches?

A. S (Secure)
B. nG (non-Global)
C. xN (Execute Never)
D. AP (Access Permission)

Answer: C

QUESTION NO: 20

An ARMv7 implementation might include the VFPv4-D32 floating point extension. What does the '32' indicate?

A. The width of the datapath in bits
B. The number of double precision floating point registers implemented
C. The number of bits of data that can be loaded or stored at once
D. The number of integer operations that can be performed simultaneously

Answer: B

QUESTION NO: 21

It is common to declare structures as "packed" in order to minimize data memory size. Which of the following accurately describes the effect of this?

A. Members will be stored as bit-fields
B. Data Aborts will be disabled for all structure accesses
C. Structure members will be re-ordered so that the smallest are first
D. Multi-byte members are not required to be naturally aligned

Answer: D

QUESTION NO: 22

When debugging an embedded Linux system, which one of the following techniques can be used to halt a single user thread, while allowing other threads to continue to run during the debug process?

A. Halting a single user thread in an embedded Linux system is not possible
B. Use the Linux kernel printk() function to output messages to the console
C. Connect a Linux-aware JTAG debugger to the target, which allows single-stepping of the code
D. Connect a debugger running on an external host device to an instance of gdbserver running on the target, using Ethernet

Answer: D

QUESTION NO: 23

Which of the following processors includes a Generic Interrupt Controller as a standard component?

A. Cortex-A8
B. Cortex-M3
C. Cortex-R4F
D. Cortex-A9 MPCore

Answer: D

QUESTION NO: 24

Assume a multicore processor with coherency management based on the MESI protocol. When a core changes the contents of a shared cache line, what is the final status of that line in the local cache?

A. Modified
B. Exclusive
C. Shared
D. Invalid

Answer: A

QUESTION NO: 25

How is data written into NOR flash memory?

A. Data can only be written once, when the flash device is being manufactured
B. Writing data to the memory locations using store instruction, as you would with RAM
C. Reading and writing specific registers following a device-specific procedure
D. Using an external programming device, which utilizes an ultra-violet lamp to alter the data stored on the device

Answer: C

QUESTION NO: 26

Under which of the following data-sharing scenarios would cache maintenance operations be necessary?

A. Sharing data with another thread running on the same core
B. Sharing data with another process running on the same core
C. Sharing data with an external device
D. Sharing data with another CPU in an SMP system

Answer: C

QUESTION NO: 27

A Just-In-Time compiler writes instructions to a region of memory that is configured using a writeback cache strategy. For the locations that have been written, what is the MINIMUM cache maintenance that MUST be performed before the new instructions can be reliably executed?

A. Instruction cache clean only
B. Instruction cache invalidate only
C. Data cache clean and instruction cache invalidate
D. Data cache invalidate and instruction cache invalidate

Answer: C

QUESTION NO: 28

Which of the following statements best describes a Board Support Package (BSP)?

A. PC interface hardware for configuring a boot monitor
B. Hardware specific source code needed for operating system support
C. A working port of Linux for a specific hardware platform
D. Debugging hardware and software supplied with a development board

Answer: B

QUESTION NO: 29

In the Generic Interrupt Controller (GIC) architecture, which of the following ID numbers are reserved for interrupts that are private to a CPU interface?

A. ID0-ID7
B. ID0-ID15
C. ID0-ID31
D. ID0-ID63

Answer: C

QUESTION NO: 30

What is the value of r0 after executing the following instruction sequence?

MOV r0, #200

MOV r5, #1

STR r3, [r0, r5, LSL#3]!

A. 200
B. 201
C. 204
D. 208

Answer: D

QUESTION NO: 31

Which of the following properties is a required characteristic of a Symmetric Multiprocessing (SMP) system?

A. All processors have the same view of memory
B. An even number of processors is included
C. All processors run in the same power state
D. All processors switch between operating system tasks in lock-step

Answer: A

QUESTION NO: 32

Which of the following techniques can be used to obtain a precise count of clock cycles when profiling software over an arbitrarily long period of time using the Performance Monitoring Unit?

A. A dedicated real-time clock to provide the total cycle count
B. Use of the divide-by 64 counting option to avoid an overflow of the cycle counter
C. Use of the overflow interrupts, to extend the range of the built-in 32-bit counter
D. Modification of the application software being profiled, to insert timestamps at regular intervals

Answer: C

QUESTION NO: 33

Which of the following is preserved in dormant mode?

A. Core register contents
B. CP15 (system) register settings
C. Debug state
D. Cache contents

Answer: D

QUESTION NO: 34

In general, when programming in C, stack accesses will be reduced by:

A. Disabling inlining.

B. Never passing more than four parameters in function calls.
C. Declaring automatic variables as "packed".
D. Configuring the compiler to optimize for space.

Answer: B

QUESTION NO: 35

Consider the following instruction sequence:

```
STR r0,  [r2]  ;  instruction A

DSB

ADD r0,  r1,  r2  ;  instruction B

LDR r3,  [r4]  ;  instruction C

SUB r5,  r6,  #3  ;  instruction D
```

At what point will execution pause until the STR access is complete?

A. After instruction A and before the DSB
B. After the DSB and before instruction B
C. After instruction B and before instruction C
D. After instruction C and before instruction D

Answer: B

QUESTION NO: 36

What is an "Entry point" in an application?

A. A place where execution can start
B. The location of the main () function
C. The lowest address contained in a program image
D. A location where the linker can store additional information

Answer: A

QUESTION NO: 37

In an ARMv7-A processor, with which level of the memory system is the Memory Management Unit (MMU) associated?

A. Level 1
B. Level 2
C. Level 3
D. Level 4

Answer: A

QUESTION NO: 38

An application contains three calls to an external function, foobar(), which is defined in a shared (or dynamic) library. How many copies of foobar() will the linker place in the application image?

(Ignore linker inlining)

A. None
B. Always one
C. Always three
D. One or more depending on optimization level

Answer: A

QUESTION NO: 39

In an MPCore system, when one core is waiting for resources to be released, what instruction could be used to reduce that core's power consumption?

A. WFE
B. PLD
C. NOP

D. DSB

Answer: A

QUESTION NO: 40

According to the AAPCS (with soft floating point linkage), when the caller "func" calls sprintf, where is the value of the parameter "x" placed?

```
#include <stdio.h>

void func(double x, int i , char *buffer)

{

sprintf(buffer, "pass %d: value = %f\n", i, x); }
```

A. Split between register R3 and 4 bytes on the stack
B. Split between registers R3 and R4
C. 8 bytes on the stack
D. VFP Register D0

Answer: C

QUESTION NO: 41

In a Cortex-A processor, assume an initial value of R1 =0x80004000.

If the following instruction causes a data abort, what value will R1 contain on entry to the abort handler?

```
LDR R0, [R1, #8]!
```

A. 0x80003FF8
B. 0x80004000
C. 0x80004008
D. R1 contents are unpredictable

Answer: B

QUESTION NO: 42

Which of the following operations would count as intrusive to normal processor operation?

A. Tracing using Embedded Trace Macrocell (ETM)
B. Halt mode debugging
C. Monitor mode debugging
D. Using the Performance Monitor Unit

Answer: B

QUESTION NO: 43

In an ARMv7-A processor that includes the Advanced SIMD extension (NEON), where are the data values operated on by NEON instructions stored?

A. In system memory
B. In registers shared with the VFP register set
C. In registers shared with the integer register set
D. In dedicated registers not shared with other registers

Answer: B

QUESTION NO: 44

Which of the following sequences of stages comprise the ARM7TDMI three-stage pipeline?

A. Fetch, Decode, Execute
B. Decode, Fetch, Execute
C. Execute, Fetch, Decode
D. Fetch, Execute, Execute

Answer: A

QUESTION NO: 45

According to the AAPCS, which of the following statements is TRUE with regard to preservation of register values by a function?

A. A function must preserve R0-R3 and R12
B. A function must preserve R4-R11 andR13
C. No registers may be corrupted by any function
D. All registers may be corrupted by any function

Answer: B

QUESTION NO: 46

An advantage of native compiling over cross compiling is that:

A. It can enable the final code to be smaller, and execute more quickly.
B. It allows greater parallelism when building code by utilizing many processors.
C. The compiler is able to produce error and warning messages in a range of languages.
D. Build scripts can detect details of the target, and automatically configure the build to match.

Answer: D

QUESTION NO: 47

An interrupt handler contains the following instruction sequence at the end. The purpose of these instructions is to clear the interrupt request in the interrupt controller and then safely re-enable interrupts.

STR r0, [r1] ; write to interrupt controller register to clear interrupt request

<x>

CPSIE i ; re-enable IRQ interrupts

Which of the following instructions should be placed at position <x> in order to ensure that the interrupt controller sees the write before interrupts are re-enabled?

A. DMB
B. DSB
C. ISB
D. NOP

Answer: B

QUESTION NO: 48

The purpose of a translation lookaside buffer (TLB) is to:

A. Protect memory.
B. Improve performance.
C. Implement virtual memory,
D. Ensure correct ordering of memory operations.

Answer: B

QUESTION NO: 49

How many bytes of stack are needed to pass parameters when calling the following function?

int foo(short arg_a, long long arg_b, char arg_c, int arg_d)

A. 0
B. 4
C. 8
D. 15

Answer: C

QUESTION NO: 50

Which one of the following statements is TRUE for software breakpoints?

A. Limited software breakpoints can be placed in code running from ROM
B. Each software breakpoint requires one watchpoint resource in the debug hardware
C. Each software breakpoint requires one breakpoint resource in the debug hardware
D. The number of available software breakpoints is not limited by the debug hardware

Answer: D

QUESTION NO: 51

Using a lower optimization level when compiling will:

A. Produce faster code.
B. Produce smaller code.
C. Produce non standard-compliant code.
D. Produce code that might be easier to debug.

Answer: D

QUESTION NO: 52

Which instruction would be used to return from a Reset exception?

A. MOVS PC, R14
B. MOVSPC, R13
C. Architecturally not defined
D. SUBS PC, R14, #4

Answer: C

QUESTION NO: 53

In a Cortex-A9 MPCore cluster with four processors, which of the processors can be interrupted by a software-generated interrupt?

A. Any processor in the cluster
B. Only the processor raising the software-generated interrupt
C. Only processors outside the cluster
D. Any processor except the one raising the software-generated interrupt

Answer: A

QUESTION NO: 54

To return from a Data Abort handler and re-execute the aborting instruction, what value should be loaded to the PC?

A. PC=LR
B. PC=LR44
C. PC=LR-4
D. PC=LR-8

Answer: D

QUESTION NO: 55

Which of the following register values would cause an unaligned access when the instruction LDRH r0, [r1] is executed?

A. R0=0x100, R1 =0x1000
B. R0=0x100, R1=0x1002
C. R0=0x101, R1=0x1002
D. R0=0x101. R1=0x1003

Answer: D

QUESTION NO: 56

Which ARMv7 instructions are recommended to implement a semaphore?

A. SWP, SWPB
B. TEQ, TST
C. STC, SBC
D. LDREX, STREX

Answer: D

QUESTION NO: 57

Within the ARMv7 architecture, which one of the following features is unique to the ARMv7-A profile?

A. Cache support
B. Privileged execution
C. The ARM instruction set
D. Virtual memory support

Answer: D

QUESTION NO: 58

When programming in C, how many bytes of stack are needed to pass parameters when calling the following function?

int foo(int arg_a, int arg_b, int arg_c)

A. 0
B. 4
C. 8
D. 12

Answer: A

QUESTION NO: 59

The following pseudocode sequence shows a flag being set to indicate that new data is ready to be read by another thread:

data = 123;

ready = true;

Assuming that the reader threads may execute on any other core of a multicore system, which of the following is the most efficient memory barrier to place between the two writes to prevent them being observed in the opposite order?

A. DSBSY
B. DSBST
C. DMBSY
D. DMBST

Answer: D

QUESTION NO: 60

On a processor supporting the Security Extensions, what sequence of operations is required to move from Non-secure User mode to Secure state?

A. This transition is not possible
B. Execution of an SMC instruction
C. Execution of an SMC instruction followed by an SVC instruction
D. Execution of an SVC instruction followed by an SMC instruction

Answer: D

QUESTION NO: 61

What architecture does the ARM11 MPCore implement?

A. ARMv6
B. ARMv6K

C. ARMv7-A
D. ARMv7-A with the Multiprocessing Extensions

Answer: B

QUESTION NO: 62

The following function is declared: float func(float fl, float f2);

The file file1 .c contains a call to func, and is compiled with hard floating point linkage. The file file2.c contains the definition of func, and is compiled with AACPS soft floating point linkage.

Assume that the two files are successfully linked using the ARM linker and an executable is generated. The generated executable:

A. Exhibits correct behavior, but suffers a performance penalty because the linker has to generate extra code.
B. Exhibits correct behavior, and suffers no performance penalty.
C. Will not execute.
D. Exhibits incorrect behavior.

Answer: D

QUESTION NO: 63

During an investigation into a software performance problem an engineer doubles the clock frequency of a cached ARM processor running the software. Unfortunately the performance of the application does not increase by very much, despite running on the processor for 100% of the time. What is likely to be the main bottleneck in the system?

A. The processor is context switching between multiple processes
B. Performance is limited by the speed of external memory
C. The processor is taking too long to execute branch instructions
D. The system is raising interrupts too fast for the processor to handle them

Answer: B

QUESTION NO: 64

In which of the following situations would you use a mutex to avoid synchronization problems?

A. A single-threaded application needs to manage two separate UART peripherals
B. Two independent threads running on a single processor both need to access a single UART
C. In a dual-core system, a UART is accessed by a single thread running on one of the processors
D. In a dual-core system, processor A needs to access UART A and processor B needs to access UART B

Answer: B

QUESTION NO: 65

Which of the following will cause the ARM Compiler to target the Thumb instruction set?

A. Compiling exception handlers
B. Specifying a Thumb-capable processor (e.g. -cpu=Cortex-A9)
C. Enabling Thumb code generation on the command line (--thumb)
D. Configuring the compiler for maximum code density (-Ospace)

Answer: C

QUESTION NO: 66

Which TWO of the following options can the ARM Compiler (armcc) directive__packed be used for? (Choose two)

A. To tell the compiler to use only Thumb code
B. To tell the compiler to produce code of minimum size
C. To tell the compiler to use the v6 SIMD pack/unpack instructions
D. To tell the compiler that an object can be on an unaligned address
E. To tell the compiler not to perform padding inside structures

Answer: D,E

QUESTION NO: 67

When using an Operating System, which of the following operations can NOT typically be done by user processes?

A. Reading the link register (R14)
B. Reading data from the user stack
C. Changing from ARM state to Thumb state
D. Changing the interrupt mask bits (A, I, F) in the CPSR

Answer: D

QUESTION NO: 68

In the ARM instruction set what is the maximum branch distance for a Branch or Branch and Link instruction?

A. ±32MB
B. ±4MB
C. ±12KB
D. ±4KB

Answer: A

QUESTION NO: 69

Which of the following ARM processors has the best energy efficiency (measured in mW/MHz)?

A. Cortex-M0+
B. Cortex-M4
C. Cortex-R4
D. Cortex-A15

Answer: A

QUESTION NO: 70

In an ARMv7-A processor with Security Extensions, which of the following mechanisms best describes the way Secure memory is protected from access by software running in a Non-secure privileged mode?

A. The memory system has visibility of the security status of all accesses, and will reject all Non-secure accesses to Secure memory
B. Secure memory contents are encrypted, and cannot be decrypted by Non-secure software
C. The level 2 cache controller blocks all accesses to Secure memory when the SCR.NS bit of the processor is set
D. The MMU generates an abort on accesses to Secure memory performed by Non-secure software

Answer: A

QUESTION NO: 71

Processors which implement the ARMv7-A architecture can be configured to allow unaligned memory access. Unaligned accesses have a number of advantages, disadvantages, and limitations.

Which TWO of the following statements are true? (Choose two)

A. Unaligned accesses may take more cycles to execute than aligned accesses
B. Unaligned loads and stores are necessary for accessing fields in packed structures
C. A program compiled using unaligned accesses can be safely executed on all ARMv7-A devices
D. If the relevant control register setting is enabled all loads and stores can function from unaligned addresses
E. Unaligned accesses can only be made to Normal memory

Answer: A,E

QUESTION NO: 72

The Cortex-A9 MPCore processor contains a hardware block whose function is to maintain data cache coherency between cores. What is the name of this block?

A. Shareable Memory
B. Snoop Control Unit
C. Private Memory Region
D. Level 2 Cache Controller

Answer: B

QUESTION NO: 73

Which TWO of the following accurately describe constraints on the location of the Tightly Coupled Memory (TCM) regions in a Cortex-R4 processor? (Choose two)

A. TCM Region A (ATCM) must be at a lower memory address than TCM Region B (BTCM)
B. TCM Region A can only be located at address 0x0
C. Both TCM regions must be placed at addresses which are aligned to their size
D. The two TCM regions may not overlap
E. TCM Region B (BTCM) must be located immediately above TCM Region A (ATCM)

Answer: C

QUESTION NO: 74

Which of the following processor resources do NOT have to be saved or modified by the Linux scheduler during context switch?

A. Registers R0-R15
B. Thread and process ID registers
C. The CPSR
D. NEON and VFP registers

Answer: D

QUESTION NO: 75

A function written in C has the prototype:

void my_function(float a. double b, float c);

The function is built and linked into an application using hard floating-point linkage. What registers are used to pass arguments to the function?

A. a->s0; b->d0; c->s1
B. a->s0; b->d1; c->s1
C. a->d0; b->d1; c->d2
D. a->s0; b->d1; c-> s2

Answer: B

QUESTION NO: 76

Under which of the following circumstances is TLB maintenance always required?

A. If a TLB miss occurs
B. On every process switch
C. If the TLB reports a fault
D. When a page table entry is changed

Answer: D

QUESTION NO: 77

Which one of the following debug methods is the least intrusive for analyzing a timing related bug?

A. Place breakpoints on strategic locations to locate the problem area
B. Instrument the code with print statements to locate the problem area
C. Use debug hardware to place watchpoints on strategic data memory locations
D. Use trace hardware to capture a trace log up to the point of the crash

Answer: D

QUESTION NO: 78

In a Cortex-A processor, after which TWO of these events is a cache maintenance operation required to ensure reliable code execution? (Choose two)

A. Processor reset
B. Switching from ARM to Thumb state
C. Changing the access permissions of a page
D. Executing a Data Memory Barrier instruction
E. Loading data from an unaligned memory address

Answer: A,C

QUESTION NO: 79

The following pair of functions implement a simple mutex spinlock which might be used to protect a critical code section in a multi-threaded application. The address of the lock variable is in r0.

```
lock_mutex:
    ldrex   r1, [r0]
    cmp     r1, #LOCKED
    <A>
    beq     lock_mutex

try_lock:
    <B>
    mov     r1, #LOCKED
    strex   r2, r1, [r0]
    cmp     r2, #0
    bne     lock_mutex
    dmb
    bx      lr

unlock_mutex:
    dmb
    <C>
    mov     r1, #UNLOCKED
    str     r1, [r0]
    dsb
    <D>
    bx      lr
```

In order to minimize power while waiting for the lock to be available. SEV and WFE instructions can be used to place the processor in a low power state while waiting for the lock to become available. At which points should these instructions be placed?

A. WFENE at <A>, SEV at <C>
B. WFEEQ at <A> SEV at <D>
C. WFE at<B> SEV at<C> WFENE at <B>
D. SEV at<D>

Answer: B

QUESTION NO: 80

Cortex-A series processors contain event counting hardware which can be used to profile and

benchmark code. The counters for these are programmed using:

A. Memory-mapped registers.
B. Generic Interrupt Controller (GIC) registers.
C. Debug Coprocessor Registers (CPU).
D. System Control Coprocessor Registers (CP15).

Answer: D

QUESTION NO: 81

When using an Operating System, which instruction is used by user code to request a service from the kernel?

A. BLX
B. RFEFD
C. SRSFD
D. SVC

Answer: D

QUESTION NO: 82

When an interrupt service routine reads the Generic Interrupt Controller (GIC) Interrupt Acknowledge Register, what state transition occurs for that interrupt ID?

A. Inactive to Active
B. Inactive to Pending
C. Active to Inactive
D. Pending to Active

Answer: D

QUESTION NO: 83

Which of the following is an accurate description of network storage as compared to on-chip RAM?

A. It has lower capacity
B. It is quicker to access
C. It is always available
D. It is easy to share with other devices

Answer: D

QUESTION NO: 84

Which TWO of the following options are DISADVANTAGES of building source code to use software floating point? (Choose two)

A. Not all floating point arithmetic operations are supported
B. Floating point calculations have lower performance than hardware floating point
C. The stack cannot be used to pass floating point function arguments
D. The results of floating point calculations will be less accurate
E. The resulting code will be larger

Answer: B,E

QUESTION NO: 85

Is it possible to use an interrupt controller based on the Generic Interrupt Controller (GIC) architecture in a device built around a single core Cortex-A9 MPCore processor?

A. No, they are completely incompatible
B. Yes, all Cortex-A9 MPCore processors include an integrated GIC
C. Yes, but a dummy second processor has to be included
D. No, a GIC is only compatible with multi-core Cortex-A9 processors

Answer: B

QUESTION NO: 86

If the processor is in User mode and then an IRQ interrupt occurs:

A. CPSR mode bits are set to User mode and SPSR _User mode bits are set to IRQ.
B. CPSR mode bits are set to IRQ and SPSR_Irq mode bits are set to User.
C. CPSR mode bits are set to IRQ and SPSR_Irq mode bits are set to IRQ.
D. CPSR mode bits are set to User and SPSR User mode bits are set to IRQ.

Answer: B

QUESTION NO: 87

The effect of clicking the Stop button in a debugger is to:

A. Put the processor(s) into debug state.
B. Force the processor to execute a BKPT instruction
C. Hold the processor in a Reset condition
D. Re-initialize the memory contents.

Answer: A

QUESTION NO: 88

In a loop termination test, how might a programmer indicate to the compiler that the loop iteration count limit is divisible by four?

A. AND the count limit with -0x3
B. Add 4 to the count limit
C. Subtract 4 from the count limit
D. Shift the count limit left two bit positions

Answer: A

QUESTION NO: 89

Which TWO of the following mechanisms cause the ARM processor to take an abort? (Choose two)

A. MPU fault
B. External memory system error
C. Bounced coprocessor instruction
D. Unrecognized instruction opcode
E. Illegal operands for a data-processing instruction

Answer: A,B

QUESTION NO: 90

An Advanced SIMD intrinsic has the prototype:

uint8xl6x2_t vld2q_u8 (uint8_t const * ptr);

How many bytes does this intrinsic load from memory?

A. 2
B. 16
C. 32
D. 256

Answer: C

QUESTION NO: 91

In which of these cases would code have better performance when compiled for Thumb state than when compiled for ARM state?

A. When the processor has no data cache
B. When the code involves many shifting operations
C. When the code has many conditionally executed instructions
D. When the processor can only fetch instructions 16-bits at a time

Answer: D

QUESTION NO: 92

What type of instruction is used for cache maintenance operations?

A. Dedicated ARM instructions
B. Dedicated Thumb instructions
C. CP14 instructions
D. CP15 instructions

Answer: D

QUESTION NO: 93

For Cortex-A series cores, what instruction(s) are recommended to implement a mutex or semaphore?

A. SWP and SWPB
B. DSB and ISB
C. LDREX and STREX
D. DMB

Answer: C

QUESTION NO: 94

An undefined instruction will cause an Undefined Instruction exception to be taken when:

A. It is fetched.
B. It is decoded.
C. It is executed.
D. It writes back its results.

Answer: C

QUESTION NO: 95

In Thumb state an ARMv7-A processor can execute:

A. Only 16-bit Thumb instructions.
B. Only 32-bit Thumb instructions.
C. 16-bit and 32-bit Thumb instructions.
D. 32-bit Thumb and certain ARM instructions.

Answer: C

QUESTION NO: 96

If a Generic Interrupt Controller (GIC) implements 64 priority levels, which priority field bits hold the priority value?

A. bits [5:0]
B. bits [7:2]
C. bits [15:10]
D. bits [31:26]

Answer: B

QUESTION NO: 97

What are the values of the NZCV bits in the CPSR after executing the following instructions?

```
LDR  R0, = 0xFFFFFFFF

ADDS  R0, R0, #1
```

A. 0101
B. 0110
C. 1001
D. 1010

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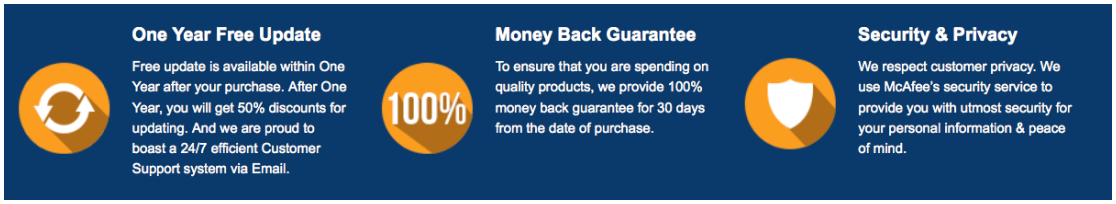

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